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EXAMINER	
THOMAS, MIA M	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/823,374	Applicant(s) VERBECK ET AL.	
	Examiner Mia M. Thomas	Art Unit 2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-21* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *10 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is made responsive to applicant's remarks received on 10 December 2007. Claims 1-15, and 17-21 are pending. Claims 1, 7, 11, 13, 14 and 15 are amended. Claim 16 is canceled. Claims 1-15 and 17-21 stand rejected.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6, 292,589 B1) in combination with Whitted et al "A Software Testbed for the Development of 3D Raster Graphics Systems" and Fuchs et al. "Pixel Planes 5: A Heterogeneous Multiprocessor Graphics System Using Processor-Enhanced Memories" ACM, Computer Graphics, Volume 23, no. 3, July 1989, pages 79-88.

Regarding Claim 1: (Currently Amended) Chow discloses a method of implementing a DCT in a GPU ("At step 442, a Discrete Cosine Transform (DCT) is applied to the block of pixels to provide image enhancement, restoration, and facilitate encoding of the image." at column 26, line 22; "FIG. 2 is a block diagram of a computer system incorporating the present invention" at column 3, line 28 which incorporates a graphics controller (Figure 2, numeral 26); comprising:

separating an image into blocks of pixels (Refer to Figure 5b; "The method includes

compressing, using the assigned quantization values, a macro block such that a resultant compressed macro block is represented by a subset of bits used to represent said macro block." at column 3, line 4);

multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels("Similarly, the order of operations is important to developing the optimal solution…by allowing IDCT and DCT to be executed in parallel." at column 45, line 36), "Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The fourth unit is a multiplier unit 678." at column 45, line 41); determining sets of scanlines based on the sets of output pixels ("The spider diagram may be read left to right and by interpreting constants above a horizontal scaling line (k1-k10) as scaling factors, and where two lines meet at a vertex a summation occurs." at column 45, line 23);

and for each set of scanlines, sampling at least a portion of the pixels comprised within the scanlines and pixels relative to the scanlines, and multiplying the sampled pixels with a row or column of the predetermined matrix ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

Fuchas teaches <u>processing</u> each block of pixels, in parallel, <u>within at least one shader module, the processing comprising</u> ("Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of

radiosity form factors. The hardware consists of up to 32 math oriented processors, up to 16 rendering units, and a conventional 1280x1024 pixel frame buffer, interconnected by a 5 gigabit ring network. Each rendering unit consists of a 128 x 128 pixel array of processors with memory with parallel quadratic expression evaluation for every pixel." at abstract; further at page 81, Section 4-"Parallel Rendering by Screen-Space Subdivision"):

Whitted teaches wherein said multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels, determining, and sampling the pixels are performed by said at least one shader module. (Refer to Figure 1, at page 44).

All these claimed elements were known methods computer designed algorithms for application of interactive 3D graphics, specifically my implementing a DCT in a GPU. The skilled artisan could have combined and/or substituted the method of processing the blocks of pixels as taught by Fuchs with the method of performing that processing in a shader module as taught by Whitted to obtain the specified claimed elements of Claim 1. The skilled artisan could have combined these claimed elements by these known methods and there would have been no change in their respective functions.

Therefore, the combination/substitution of these claimed elements would have yielded predictable results to one of ordinary skill in the art at the time of the invention. The combination of the disclosure of Chow in view of Whitted and Fuchs would have obtained the specified claim elements of Claim 1 are thereby obvious. Additionally, "shaders profoundly affect the realism that can be achieved in computer generated images." (Whitted, page 43, paragraph 2 under subsection "Design Philosophy").

For clarity, the processor of Fuchs as stated at page 81, Section 4, “Parallel Rendering by Screen-Space Subdivision”; the author details “that the parallel processing that occurs is rendered on a pixel-pixel basis.” (Further at pages 81, paragraph 1-6). The substitution of this form of processing meets the limitation of processing each block of pixels, in parallel. The combination of Fuchs with Whitted also meets the limitation of processing within at least one shader module. Therefore, the combination of these forms of processing (Fuchs and Whitted) and further in combination with Chow makes these claims obvious to the skilled artisan to make and combine to yield predictable results.

Regarding Claim 2: (Previously presented) Chow discloses the multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels, determining, and sampling the pixels are performed in the GPU (“Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The first is the double buffer operand store 646. The second and third functional units are adders 676 and 677. Each adder has four associated scratchpad registers 675. These registers are 2 write/2 read port registers. Each adder is capable of performing 2's complement addition or subtraction. The fourth unit is a multiplier unit 678.” at column 45, line 41).

Regarding Claim 3:(Original) Chow discloses each corresponding set of output pixels corresponds to a textured line across the pixels in the blocks of pixels (Referring to Figure 19(b) and Figure 21, the macroblock templates to be inputted are considered at step 464 (Figure 21),

bi directional which resolves that the output pixels will correspond to a textured line across the pixels).

Regarding Claim 4:(Original) Chow discloses wherein sampling the pixels comprised within the scanlines comprises using a separate shader for each set of scanlines (Referring to Figures 6(a)-6(c); "Referring briefly to FIGS. 6A and 6B, the motion estimation process will be described with reference to a series of frames 60. Each frame of the series 60 includes pixels designated via (x, y) coordinates…"As seen in FIG. 6B, motion estimation is shown to include 3 discrete steps; a block matching step 66, a motion vector generation step 67 and an energy calculation step 68. Block-matching techniques are used to identify macro blocks in the preceding (and/or succeeding) frames, which have the best match of pixel values to the macroblock of interest in the current frame. The macroblock matching procedure may be performed using a series of adder circuits or other methods apparent to those in the art." at column 10, line 18).

Regarding Claims 5: (Original) Chow discloses defining an array of coordinate offsets to neighboring pixels, wherein the shader accesses the pixels in the scanlines using the offset array ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

Regarding Claims 6:(Original) Chow discloses the same shader can be used for each pixel in a scanline ("The DFU is responsible for reducing the amount of video data by means of sub-sampling and decimation of horizontal scan lines as they arrive by optionally keeping only half the scan lines, either even or odd." at column 7, line 28; The hardware or circuit used to

perform the DCT transform must be made as fast and as simple as possible. It is highly desirable to use the same physical logic gate for as many parts of the transform as possible, since to do so results in the fewest number of transistors needed to perform the operation. The fewer the number of transistors used, the faster and more economical the circuit will be." at column 45, line 66).

Regarding Claim 7 (Currently Amended) Chow discloses a method of processing pixels, comprising: separating an image into blocks of pixels (Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4);

performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); and
creating a line for each row or column in each block of pixels, ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); wherein the rows or columns correspond to the polylines created for each column or row; ("The spider diagram may be read left to right and by interpreting constants above a horizontal scaling line (k1-k10) as scaling factors, and where two lines meet at a vertex a summation occurs." at column 45, line 23);

Fuchas teaches <u>processing </u>each block of pixels, in parallel, <u>within at least one shader module,</u> ("Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form factors. The

hardware consists of up to 32 math oreiented processors, up to 16 rendering units, and a conventional 1280x1024 pixel frame buffer, interconnected by a 5 gigabit ring network. Each rendering unit consists of a 128 x 128 pixel array of processors with memory with parallel quadratic expression evaluation for every pixel." at abstract; further at page 81, Section 4- "Parallel Rendering by Screen-Space Subdivision"):

creating a polyline of pixels for each column or row in each block of pixels ("The 8x8 2-D DCT is

Whitted teaches wherein said creating a polyline and creating a line are performed by <u>said at least</u> one shader module (Refer to Figure 1, at page 44).

All these claimed elements were known methods computer designed algorithms for application of interactive 3D graphics, specifically my implementing a DCT in a GPU. The skilled artisan could have combined and/or substituted the method of processing the blocks of pixels as taught by Fuchs with the method of performing that processing in a shader module as taught by Whitted to obtain the specified claimed elements of Claim 7. The skilled artisan could have combined these claimed elements by these known methods and there would have been no change in their respective functions.

Therefore, the combination/substitution of these claimed elements would have yielded predictable results to one of ordinary skill in the art at the time of the invention. The combination of the disclosure of Chow in view of Whitted and Fuchs would have obtained the specified claim elements of Claim 7 are thereby obvious. Additionally, "shaders profoundly affect the realism

that can be achieved in computer generated images." (Whitted, page 43, paragraph 2 under subsection "Design Philosophy").

For clarity, the processor of Fuchs as stated at page 81, Section 4, "Parallel Rendering by Screen-Space Subdivision"; the author details "that the parallel processing that occurs is rendered on a pixel-pixel basis." (further at pages 81, paragraph 1-6). The substitution of this form of processing meets the limitation of processing each block of pixels, in parallel. The combination of Fuchs with Whitted also meets the limitation of processing within at least one shader module. Therefore, the combination of these forms of processing (Fuchs and Whitted) and further in combination with Chow makes these claims obvious to the skilled artisan to make and combine to yield predictable results.

Regarding Claim 8: (Original) Chow discloses creating a polyline of pixels for each row or column in each block of pixels ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20); and creating a line for each column or row in each block of pixels, wherein the rows or columns correspond to the polylines created for each row or column (Refer to Figure 32; "FIG. 32 illustrates a partitioning of a block of video data into left and right halves for row transforms, and into top and bottom halves for column transforms, for purposes of the DCT operation of FIG. 31" at column 4, line 52).

Regarding Claim 9 (Original) Chow discloses determining sets of scanlines based on the lines created for each row or column in each block of pixels; and for each set of scanlines, sampling the pixels comprised within the scanlines and multiplying the sampled pixels with a row or

column of a predetermined matrix ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

Regarding Claim 10: (Original) Chow discloses the steps of creating are performed in a graphics processing unit (GPU) (Referring to Figure 28, numeral 20 (PCI Local Bus), the portion of Figure 28 allows the graphics controller (26) of Figure 2 to show that it is connected to the PCI Local bus).

Regarding Claim 11: (Currently Amended) Chow discloses a method of processing pixels, comprising: separating an image into blocks of pixels (Refer to Figure 5b; "The method includes compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4);

determining a polyline of pixels for each column or row in each block of pixels ("The 8x8 2-D DCT is performed by evaluating the eight 1-D row transforms, then evaluating these results through 8 column transforms." at column 45, line 20);
for each pixel in the polyline, sampling at least a portion of the other pixels in the corresponding column or row that lies along the polyline and pixels relative to the column or row ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).
multiplying each of the other pixels by a DCT coefficient from a predetermined matrix to generate resultant values; and adding the resultant values together to generate a resulting value

("Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The fourth unit is a multiplier unit 678." at column 45, line 41);

Whitted teaches wherein said multiplying and adding are performed by <u>said at least one </u>shader module (Refer to Figure 1, at page 44, block labeled "Transformations…").

Fuchas teaches <u>processing each block within at least one shader module:</u> ("Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form factors. The hardware consists of up to 32 math oriented processors, up to 16 rendering units, and a conventional 1280x1024 pixel frame buffer, interconnected by a 5 gigabit ring network. Each rendering unit consists of a 128 x 128 pixel array of processors with memory with parallel quadratic expression evaluation for every pixel." at abstract; further at page 81, Section 4-"Parallel Rendering by Screen-Space Subdivision"):

All these claimed elements were known methods computer designed algorithms for application of interactive 3D graphics, specifically my implementing a DCT in a GPU. The skilled artisan could have combined and/or substituted the method of processing the blocks of pixels as taught by Fuchs with the method of performing that processing in a shader module as taught by Whitted to obtain the specified claimed elements of Claim 11. The skilled artisan could have combined these claimed elements by these known methods and there would have been no change in their respective functions.

Therefore, the combination/substitution of these claimed elements would have yielded predictable results to one of ordinary skill in the art at the time of the invention. The combination of the disclosure of Chow in view of Whitted and Fuchs would have obtained the specified claim elements of Claim 11 are thereby obvious. Additionally, "shaders profoundly affect the realism that can be achieved in computer generated images." (Whitted, page 43, paragraph 2 under subsection "Design Philosophy").

For clarity, the processor of Fuchs as stated at page 81, Section 4, "Parallel Rendering by Screen-Space Subdivision"; the author details "that the parallel processing that occurs is rendered on a pixel-pixel basis." (further at pages 81, paragraph 1-6). The substitution of this form of processing meets the limitation of processing each block of pixels, in parallel. The combination of Fuchs with Whitted also meets the limitation of processing within at least one shader module. Therefore, the combination of these forms of processing (Fuchs and Whitted) and further in combination with Chow makes these claims obvious to the skilled artisan to make and combine to yield predictable results.

Regarding Claim 12: (Original) Chow discloses biasing and scaling at least one of the polyline of pixels, the resultant values, and each resulting value for each pixel ("Prior to writing the row or column results into the double buffer 646, each result must be rounded via an incrementer 681, which is a non-biased two's complement rounding unit." at column 45, line 51).

Regarding Claim 13:(Currently Amended) Chow discloses a method of processing pixels comprising: separating an image into blocks of pixels (Refer to Figure 5b; "The method includes

compressing, using the assigned quantization values, a macroblock such that a resultant compressed macroblock is represented by a subset of bits used to represent said macroblock." at column 3, line 4); for each column in a block of pixels, setting up a shader and rendering a scanline; and for each row in a block of pixels, setting up a shader and rendering a column; (Referring to Figures 6(a)-6(c); "Referring briefly to FIGS. 6A and 6B, the motion estimation process will be described with reference to a series of frames 60. Each frame of the series 60 includes pixels designated via (x, y) coordinates…"As seen in FIG. 6B, motion estimation is shown to include 3 discrete steps; a block matching step 66, a motion vector generation step 67 and an energy calculation step 68. Block-matching techniques are used to identify macroblocks in the preceding (and/or succeeding) frames, which have the best match of pixel values to the macroblock of interest in the current frame. The macroblock matching procedure may be performed using a series of adder circuits or other methods apparent to those in the art." at column 10, line 18);

Whitted teaches <u>and wherein the setting up and the rendering are performed by said at least one shader module</u> (Refer to Figure 1, at page 44, block labeled "Transformations…").

Fuchas teaches <u>processing each block within at least one shader module:</u> ("Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form factors. The hardware consists of up to 32 math oriented processors, up to 16 rendering units, and a conventional 1280x1024 pixel frame buffer, interconnected by a 5 gigabit ring network. Each rendering unit consists of a 128 x 128 pixel array of processors with memory with parallel quadratic expression evaluation

for every pixel." at abstract; further at page 81, Section 4-"Parallel Rendering by Screen-Space Subdivision"):

All these claimed elements were known methods computer designed algorithms for application of interactive 3D graphics, specifically my implementing a DCT in a GPU. The skilled artisan could have combined and/or substituted the method of processing the blocks of pixels as taught by Fuchs with the method of performing that processing in a shader module as taught by Whitted to obtain the specified claimed elements of Claim 13. The skilled artisan could have combined these claimed elements by these known methods and there would have been no change in their respective functions.

Therefore, the combination/substitution of these claimed elements would have yielded predictable results to one of ordinary skill in the art at the time of the invention. The combination of the disclosure of Chow in view of Whitted and Fuchs would have obtained the specified claim elements of Claim 13 are thereby obvious. Additionally, "shaders profoundly affect the realism that can be achieved in computer generated images." (Whitted, page 43, paragraph 2 under subsection "Design Philosophy").

For clarity, the processor of Fuchs as stated at page 81, Section 4, "Parallel Rendering by Screen-Space Subdivision"; the author details "that the parallel processing that occurs is rendered on a pixel-pixel basis." (further at pages 81, paragraph 1-6). The substitution of this form of processing meets the limitation of processing each block of pixels, in parallel. The combination of Fuchs with Whitted also meets the limitation of processing within at least one shader module. Therefore, the combination of these forms of processing (Fuchs and Whitted)

and further in combination with Chow makes these claims obvious to the skilled artisan to make and combine to yield predictable results.

Regarding Claim 14:(Currently Amended) Chow discloses setting up the shaders and the rendering are performed in the GPU (Referring now to FIG. 2, a computer system 10 for use with the present invention is shown to include a central processing unit (CPU) 12…Also coupled to the PCI bus is a graphics controller 26…" at column 5, line 44).

Regarding Claim 15: (Currently Amended) Chow discloses a system to program a GPU to implement a DCT, (Referring to Figure 2, numeral 26 (Graphics controller) and "At step 442, a Discrete Cosine Transform (DCT) is applied to the block of pixels to provide image enhancement, restoration, and facilitate encoding of the image." at column 26, line 22), comprising: adapting a processing unit to receive blocks of pixels into which an image has been separated, (Referring to Figure 28, numeral 20 (PCI Local Bus), the portion of Figure 28 allows the graphics controller (26) of Figure 2 to show that it is connected to the PCI Local bus); ("Similarly, the order of operations is important to developing the optimal solution…by allowing IDCT and DCT to be executed in parallel." at column 45, line 36)
multiplying a column or row of pixels of an image with a predetermined matrix to generate a corresponding set of output pixels("Referring now to FIG. 31A, the above described approach to DCT and IDCT computing can be provided via the DCT Unit data path implementation 674, which is shown to include 4 functional units. The fourth unit is a multiplier unit 678." at column 45, line 41);
determining sets of scanlines based on the sets of output pixels(Referring to Figure 33, numeral 651(RAM Address Wordline; "Here, the coefficients are stored using the specific ordering and

location in structure 720 to support transformation of the 8.times.8 pixel array of FIG. 32." at column 47, line 36); and

for each set of scanlines, sampling the pixels comprised within the scanlines and multiplying the sampled pixels with a row or column of the predetermined matrix (Referring to Figure 33, DCT Double Buffer Addressing; Operands 0 and 7 are found stored on address line 0 in diagram 651, with operand 0 on the left half and operand 7 on the right half, the same order as was found for operands 2 and 5." At column 48, line 10);

Whitted teaches and wherein said setting up and the rendering are performed by said at least one shader module (Refer to Figure 1, at page 44, block labeled "Transformations…").

Fuchas teaches processing each block of pixels, in parallel, by within at least one shader module ("Techniques are described for volume rendering at multiple frames per second, font generation directly from conic spline descriptions, and rapid calculation of radiosity form factors. The hardware consists of up to 32 math oriented processors, up to 16 rendering units, and a conventional 1280x1024 pixel frame buffer, interconnected by a 5 gigabit ring network. Each rendering unit consists of a 128 x 128 pixel array of processors with memory with parallel quadratic expression evaluation for every pixel." at abstract; further at page 81, Section 4- "Parallel Rendering by Screen-Space Subdivision"):

All these claimed elements were known methods computer designed algorithms for application of interactive 3D graphics, specifically my implementing a DCT in a GPU. The skilled artisan

could have combined and/or substituted the method of processing the blocks of pixels as taught by Fuchs with the method of performing that processing in a shader module as taught by Whitted to obtain the specified claimed elements of Claim 13. The skilled artisan could have combined these claimed elements by these known methods and there would have been no change in their respective functions.

Therefore, the combination/substitution of these claimed elements would have yielded predictable results to one of ordinary skill in the art at the time of the invention. The combination of the disclosure of Chow in view of Whitted and Fuchs would have obtained the specified claim elements of Claim 13 are thereby obvious. Additionally, “shaders profoundly affect the realism that can be achieved in computer generated images.” (Whitted, page 43, paragraph 2 under subsection “Design Philosophy”).

For clarity, the processor of Fuchs as stated at page 81, Section 4, “Parallel Rendering by Screen-Space Subdivision”; the author details “that the parallel processing that occurs is rendered on a pixel-pixel basis.” (further at pages 81, paragraph 1-6). The substitution of this form of processing meets the limitation of processing each block of pixels, in parallel. The combination of Fuchs with Whitted also meets the limitation of processing within at least one shader module. Therefore, the combination of these forms of processing (Fuchs and Whitted) and further in combination with Chow makes these claims obvious to the skilled artisan to make and combine to yield predictable results.

Regarding Claim 16: (Canceled)

Regarding Claim 17: (Previously presented) Chow discloses a CPU coupled to the GPU by a system bus, the CPU capable of separating the image into the blocks of pixels (Referring now to FIG. 2, a computer system 10 for use with the present invention is shown to include a central processing unit (CPU) 12…Also coupled to the PCI bus is a graphics controller 26…" at column 5, line 44).

Regarding Claim 18: (Previously presented) Chow discloses the system that equally resembles the method of claim 3. Claim 18 standing rejected for the same reasoning's as stated at Claim 3.

Regarding Claim 19: (Previously presented) Chow discloses the GPU comprises a separate shader for sampling the pixels comprised within each set of the scanlines ("Raw, analog video data are received by the color decoder 33 …according to the CCIR601 standard at either an NTSC format of 720 pixels x 480 scan lines at 29.97 frames/second, or PAL format of 720 pixels x 576 lines at 25 frames per second." At column 6, line 18).

Regarding Claim 20: (Original) Chow discloses the GPU defines an array of coordinate offsets to neighboring pixels, wherein the shader accesses the pixels in the scanlines using the offset array ("Here, the coefficients are stored using the specific ordering and location in structure 720 to support transformation of the 8 x 8 pixel array of FIG. 32." at column 47, line 36).

Regarding Claim 21: (Original) Chow discloses the same shader can be used for each pixel in a scanline ("The DFU is responsible for reducing the amount of video data by means of sub-

sampling and decimation of horizontal scan lines as they arrive by optionally keeping only half the scan lines, either even or odd." at column 7, line 28; The hardware or circuit used to perform the DCT transform must be made as fast and as simple as possible. It is highly desirable to use the same physical logic gate for as many parts of the transform as possible, since to do so results in the fewest number of transistors needed to perform the operation. The fewer the number of transistors used, the faster and more economical the circuit will be." at column 45, line 66).

Response to Arguments

4. Applicant's arguments with respect to claims 1-21 have been fully considered but are moot in view of the new ground(s) of rejection.

Summary of Response: The recitations in the claims are not simply in reference to a shader, but to what processing is occurring within the shader as a part of the overall process. As what is claimed in the amended claim 1 "within at least one shader module" (see remarks page 7 last paragraph).

Examiner's Response: Reference Fuchs is replied upon to meet the deficiency of the processing occurring in the shader module already performed by Whitted in combination with Chow. Fuchs teaches the processing by way of an algorithm that is provided and techniques disclosed for implementing that algorithm. Therefore, the combination of the previously rejected claimed elements meets the limitations of each of the independent claims as stated in this instant application. Specifically, at the abstract Fuchs teaches that the rendering creates rapid calculation and the processing is performed in parallel with the pixel by pixel evaluation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mia M. Thomas whose telephone number is (571)270-1583. The examiner can normally be reached on Monday-Thursday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on 571-272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mia M Thomas/
Examiner, Art Unit 2624

/Vikkram Bali/

Supervisory Patent Examiner, Art Unit 2624